Super Testchip Methodology - Prototyping testchips for SerDes IPs

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Agenda

- Introduction – Typical SerDes Testchip
- Process to build testchip
- Challenges
- State-of-the-art solution – Super Testchip
  - Floor plan
  - Image , Package and Board
  - Testsite Logic Development , Clocking structure
- Super Testchip Methodology – TAT
- Evidence - Results & Summary
- Acknowledgements & References

Introduction - Typical SerDes Testchip

- Testchip : Qualification vehicle for the internally developed IP cores.
- Complete IP cores characterization.
- Demonstration of IP features to customers.

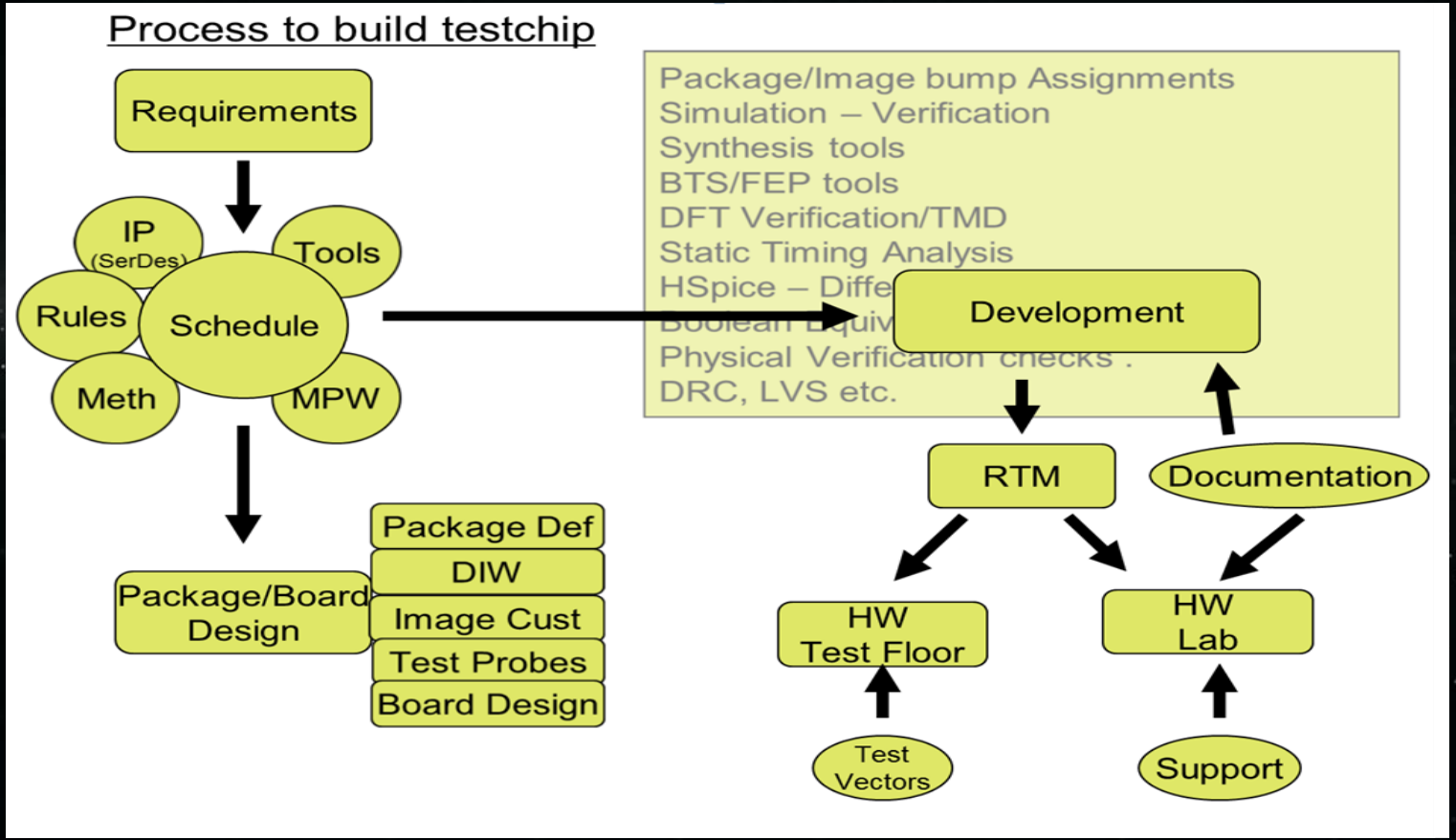
MOTIVATION

Multiple functional features like protocol specific macros, blocks/partitions, register read/writes etc are common across SerDes testsites. Reusability of these features can reduce the effort and time spent while building the testchip.

OBJECTIVE

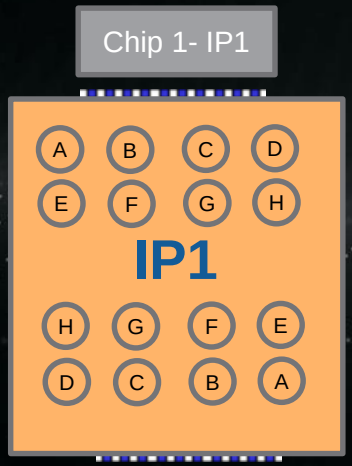
Develop a super set logic with parameterized variables, which can be programmed by the testsite developer to generate the required SerDes testchip design

How we build it ?

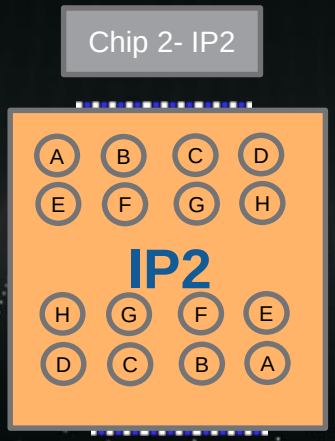


Challenges in Testchip design

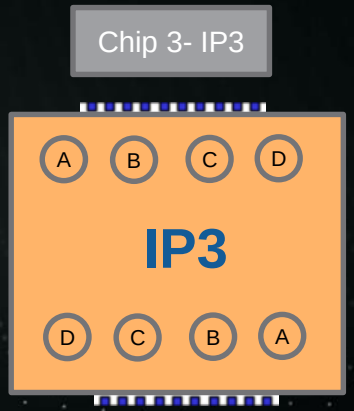
- Multiple testchips riding on a single shuttle
- Development cost



- Two Full Duplex Cores (IP1)
- IP1 size : X um x Y um
- Differential Clock Receiver
- Sinusoidal Jitter tolerance IPs
- BIST Data Generator/Checker IPs – 16/32/64/128 bit modes
- No At Speed Test (ASST) support
- MAC layer protocol supported soft IPs
- Error Correction soft IPs – Core level



- Two Full Duplex Cores (IP2)
- IP2 size : X um x Z um
- Differential Clock Receiver
- Customer logic IP
- BIST Data Generator/Checker IPs – 16/32/64/128 bit modes
- At Speed Test (ASST) support
- MAC layer protocol supported soft IPs
- Error Correction soft IPs – Core level

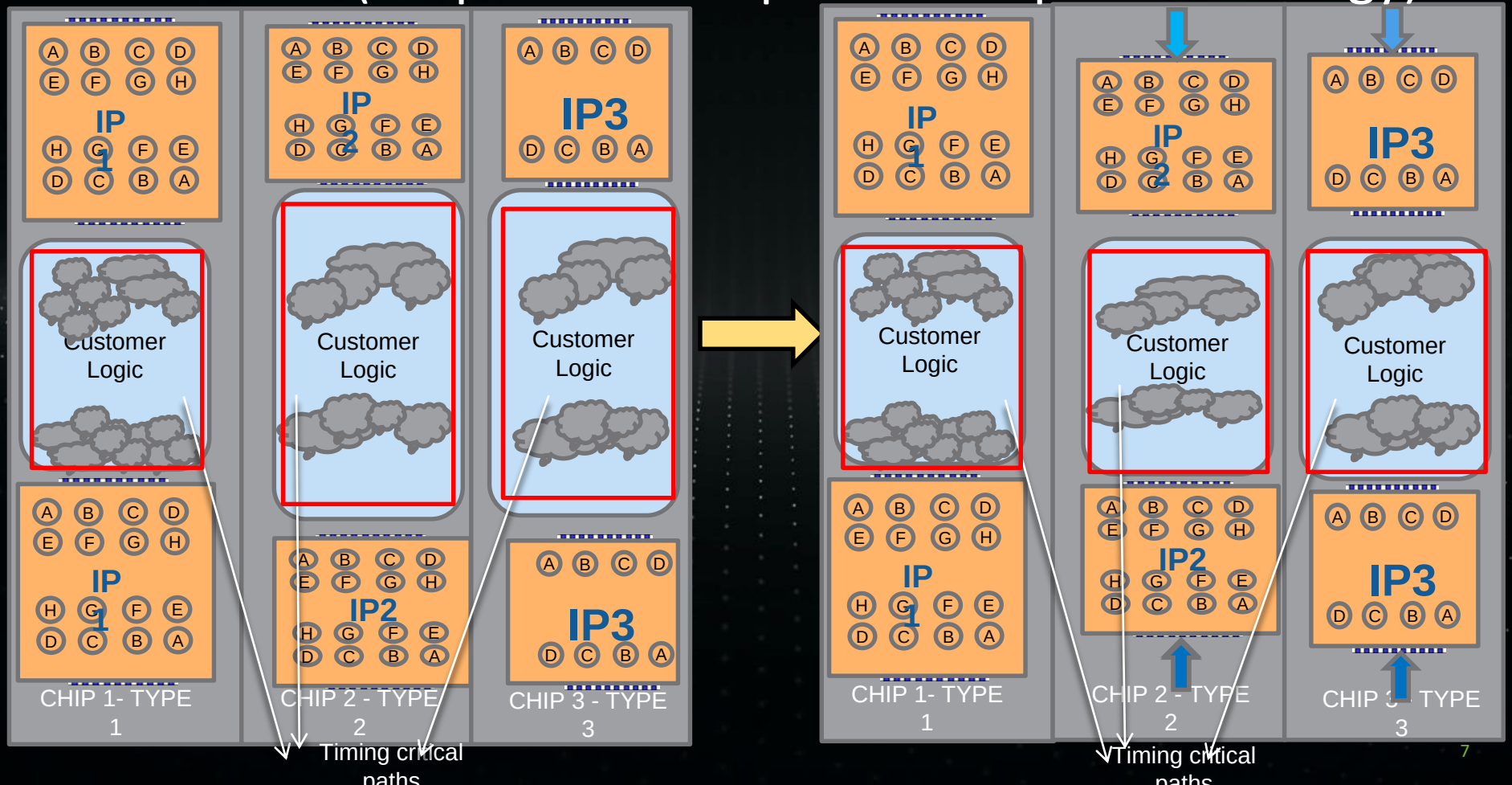


- Two Full Duplex Cores (IP3)
- IP3 size : M um x N um
- Differential Clock Receiver
- Customer logic IP
- BIST Data Generator/Checker IPs – 16/32/64/128 bit modes
- At Speed Test (ASST) support
- MAC layer protocol support IPs
- Error Correction soft IPs – Link level

A state-of-the-art solution – Super Testchip

1. Floor Plan (Proposed for Super-Testchip methodology)
2. Chip Images & Packages are different for each SerDes Testchip
3. Testchip logic development/ Integration

1. Floor Plan (Proposed for Super-Testchip methodology)



A state-of-the-art solution – Super Testchip Contd.,

2. Chip Images & Packages are different for each SerDes testsite.

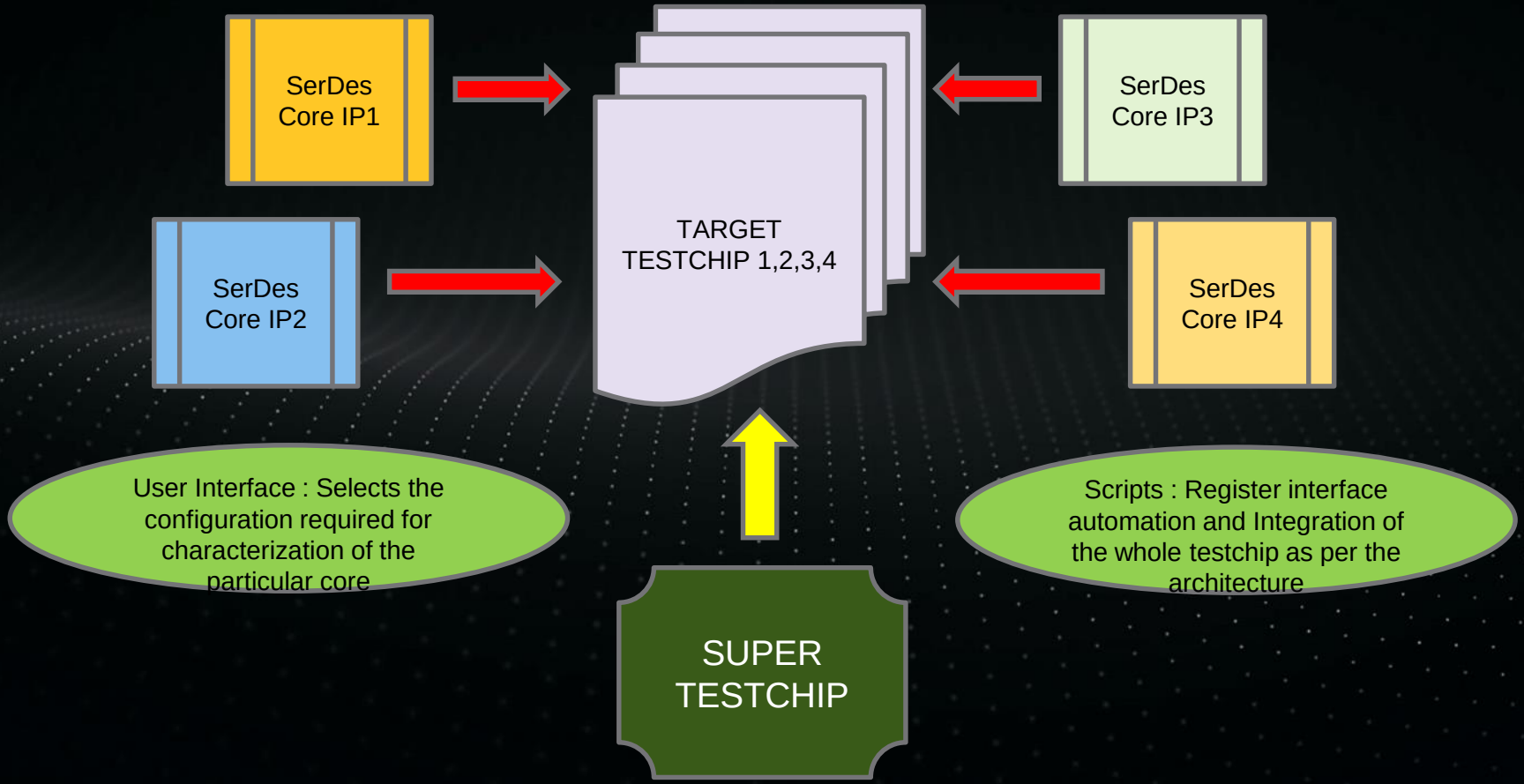
Image /Package/Board Reusability to be adopted.

- ✓ Image for n-instances of X-port cores which should support n-instances of Y-port cores as well
- ✓ Define & design additional spare Chip IOs
- ✓ Enables to have more Ball Grid Array(BGA)s to accommodate new features

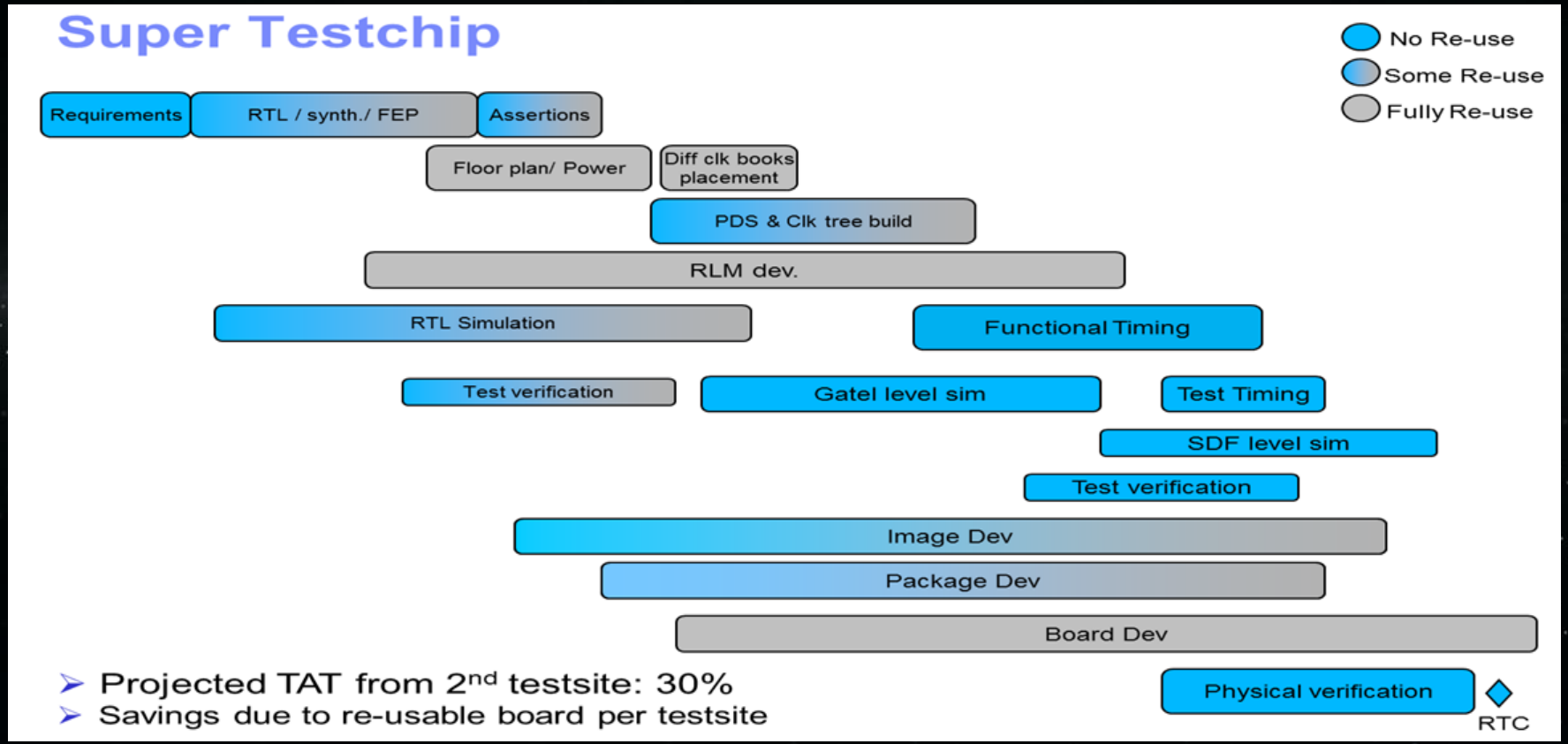
3. Testchip logic development/ Integration

- ✓ **Script based register map design & Chip integration**
  - ✓ **Enables commonality across testsites register maps**
  - ✓ More time for design reviews resulting in reduction of design bugs
- ✓ Consolidate all Sub-block/partition logic requirements
  - ✓ Customer Logic IPs
  - ✓ Create common assertion templates

A state-of-the-art solution – Super Testchip Contd.,



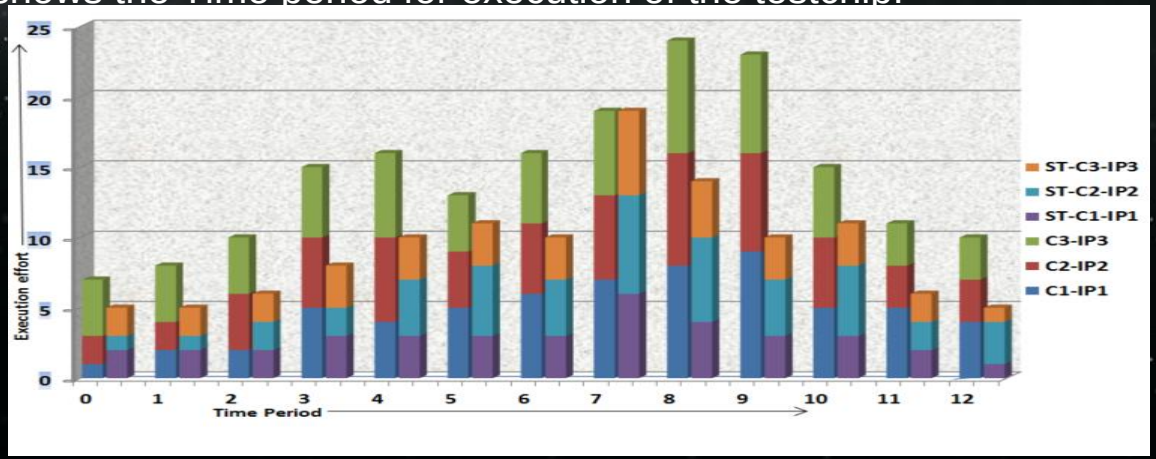
Super Testchip Methodology



Evidence

Comparision of Traditional Methodology *vs* Super Testchip Methodology

- The bar graph is shown below for 3 testchips that were released on Multi Part Wafer(MPW) recently. Both the methodologies are compared here w.r.to resources consumed in terms of people, tool runtimes and cpu usage.
- The x-axis shows the normalized effort involved for building testchip.
- The y-axis shows the Time period for execution of the testchip.



C1-IP1,C2-IP2,C3-IP3 - Names of testchips done by Traditional Methodology
ST-C1-IP1,ST-C2-IP2,ST-C3-IP3 - Names of testchips done by Super Testchip Methodology

Thank you

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